IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 26 with the following:

A typical constant ON-time controller for a buck regulator is shown in Figure 5. The output voltage (Vout) 516 is set by a duty cycle that is defined as the ratio of ON-time of the high-side field effect transistor (FET) 507 to the total switching period. Whenever Vout 516 drops below the reference voltage Vref 517, comparator 508 sets latch 509. Gate drivers ~~500~~ 508 turn FET 507 ON thereby charging inductor (L) 504 and delivering current to the load (not shown) coupled to Vout 516. Latch 509 remains set until the voltage 518 across capacitor (C) 511 exceeds Vref 517. At this time, comparator 510 resets latch 509 and gate drivers 500 turn FET 507 OFF and FET 506 ON. The energy stored in L 504 causes the load current to continue to flow to Vout 516. Catch diode (D) 505 insures current in L 504 is not interrupted during switching to minimize transients.

Please replace the paragraph beginning on page 3, line 21 with the following:

Figure 1A is a simplified block diagram of a dual phase buck regulator with constant ON-time control and active current sharing. The output capacitor (C) ~~101~~ 102 is usually a network of many capacitors in parallel. The equivalent series resistance (ESR) represented by resistor ESR ~~102~~ 101 is the effective series resistance of this capacitor network. ESR ~~102~~ 101 is the real part of the complex impedance of the network of parallel capacitors making up C ~~101~~ 102. Two sense resistors, R 137 and R 103, provide voltages VR2 127 and VR1 122 that are proportional to the ~~inductor~~ current in inductors 117 and 104 in each phase, respectively. VR1 122 is the difference in potential between node 124 and Vout 130 and VR2 127 is the difference between node 131 and Vout 130. The four field effect transistors (FETs), FET 106, FET 107, FET 116, and FET 118 control the duty cycle of each phase. Diodes 105 and 115 are flyback diodes that insure the currents in the inductors 104 and 117, respectively, are not interrupted. The gate drivers 119 and 120 in phase drive circuits 180 and 181 interface with the control circuit

121 and provide the voltages needed to drive FETs 106, 107, 116 and 118. The control circuit 121 determines which of the two phases, 180 or 181, to turn ON when the output voltage (Vout) 130 falls below the reference voltage (Vref) 123. The output currents IL1 141 and IL2 142 combine to provide load current Iout 160 to load 140.

Please replace the paragraph beginning on page 4, line 11 with the following:

Figure 2 is a circuit diagram of an open loop constant ON-time buck controller for dual converters. The output 240 of the comparator 229 is coupled to an input of AND gates 230 and 231. The outputs 241 and 242 of flip flop (FF) 228 are coupled to the other inputs of AND gates 230 and 231 respectively. Outputs 241 and 242 alternately turn ON each converter phase (280 and 281) when Vout 250 drops below the reference voltage (Vref) 217. The pulse circuits 225 and 226 and OR gate 227 provide the clock to the FF 228. FF 228 is configured as a "D-type" FF that changes state on each positive clock edge (of its CLK input). Therefore, since each pulse from pulse circuits 225 and 226 are logic ORed in OR gate 227 to form clock 252, each pulse causes outputs 241 and 242 of FF 228 to switch states. When output 242 is logic one, AND gate 231 is enabled and latch 220 in the converter phase 281 is set when the output of comparator 229 (coupled to 240) transitions to logic one. When latch 220 is set, FET 218 turns ON (via gate drivers 219) charging inductor L ~~217~~ 227 and providing current to Vout 250. Conversely, if output 241 is logic one, then AND gates 230 is enabled and latch 209 in converter phase 280 is set when the output of comparator 229 transitions to logic one turning ON FET 207 (via gate drivers 208) charging inductor L 204 and providing current to Vout 250. Latches 209 and 220 are reset by comparators 210 and 221 when the voltages on capacitors 211 and 222, respectively, exceed Vref 217. Capacitors 211 and 222 are discharged by FETs 212 and 224. Sense resistors 203 and 245 are used to sense the current in inductors 204 and 227, respectively. FETs 206 and 216 and diodes 205 and 225 insure the currents in the charging inductors are not interrupted. Capacitor 201 is the load filter capacitor and resistor 202 represents its ESR.

Please replace the paragraph beginning on page 5, line 20 with the following:

Figure 3 is a circuit diagram of circuit 300 that has the function of a closed loop average current sharing constant ON-time buck converter. The output 340 of the comparator 329 is coupled to one input AND gates 330 and 331. The outputs of flip flop (FF) 328 are coupled to positive edge delay circuits 388 and 389. Positive edge delay circuits 388 and 389 delay the rising edges of outputs 341 and 342 which in turn alternately turn ON each converter phase when Vout 350 drops below the reference voltage (Vref) 317. Pulse circuit 325 receives ON-time pulse (HSON1 385) from latch 309. Pulse circuit 326 receives ON-time pulse (HSON2 386) from latch 320. HSON1 385 and HSON2 386 are logic ORed in OR gate 327 to provide the clock to the FF 328. FF 328 is configured as a "D-type" FF that changes state on each positive clock edge. Therefore, since each pulse from pulse circuits are logic ORed in OR gate 327 to form clock 352, each pulse causes the outputs of FF 328 to switch states. When output 341 is logic one, AND gate 330 is enabled and latch 320 in the converter phase 381 is set when the comparator 329 transitions to logic one. When latch 320 is set, FET 318 turns ON charging inductor L ~~317~~ 327 and providing current to Vout 350. Conversely, if output 342 is logic one, then AND gate 331 is enabled and latch 309, in converter phase 380, is set when the output of comparator 329 transitions to logic one.

Please add the following new paragraph to explain components designated in Figure 3:

Diodes 306 and 325 insure the currents in inductors 304 and 327 are not interrupted during switching. Load filter capacitor 301 has ESR 302. Gate drivers 308 and 319 provide drive voltages to FETS 305, 307, 316 and 318. FETs 213 and 324 discharge capacitors 311 and 322 in response to reset signals from latches 309 and 320 generated when the voltages of capacitors 311 and 322 exceed Vref 317 and the outputs of comparators 310 and 321 transition to a logic one.

Please replace the paragraph beginning on page 11, line 14 with the following:

Figure 4A is a circuit diagram of a two-phase converter 400 with peak current sharing and constant ON-time control according to embodiments of the present

invention. Phase selection logic (PSL) 482 receives voltage reference (Vref) 417, Vout 450, ON-time pulse for converter phase 480 (HSON1 485) and the ON-time pulse for converter phase 481 (HSON2 486) and generates a start signal for converter phase 480 (Start PH1 490) and a start signal for converter phase 481 (Start PH2 491). Load filter capacitor 401 coupled to output 450 has corresponding ESR 402.

Please replace the paragraph beginning on page 12, line 9 with the following:

GMA 432 and GMA 434 each sense the voltage across their corresponding sense resistors R 403 and R 437. GMA 432 and GMA 434 generate currents IR 470 and IR 471, respectively. IR 470 flows through resistor R 436 generating voltage (V) 472 and IR 471 flows through R 435 generating voltage V 473. V 472 and V 473 are proportional to the voltage drops across their corresponding sense resistors R 403 and R 437. Appropriate differential amplifiers may also be used in place of GMA 432 and GMA 434. V 473 is proportional to the real-time current in converter phase 481 and is coupled directly to the positive input of GMA 433. Voltage V 472 is coupled to the sample and hold circuit formed by FET switch 439 and capacitor C 438. Due to out of phase switching, the peak current in converter phases 480 and 481 occur at different times. Therefore, the sample and hold circuit comprising FET switch 439 and C 438 samples the voltage across R 436. FET switch 439 is turned OFF (by signal 487) when the high-side FET 407 turns OFF. Thus, C 438 holds the peak voltage across R 436 corresponding to the peak current in inductor L 404. When converter phase 481 turns ON, the peak voltage (corresponding to the peak current) from converter phase 480 is compared to the real-time voltage across R 435 (corresponding to the current in L ~~417~~ 427). When the voltage across R 435 is greater than the voltage on C 438, the comparator 433 resets the latch 420 ending HSON2 486.

Please replace the paragraph beginning on page 13, line 8 with the following:

The following describes an initial ramp up of Vout 350 for dual converters 400. In Figure 4, converter phase 480 has input voltage Vin1 415 and converter phase 481 has input voltage Vin2 ~~470~~ 476. Input voltages Vin1 415 and Vin2 476 are not necessarily

equal and may be unregulated or may be from regulated sources with voltage levels that are higher than desired for Vout 450. At a start up condition, Vref 417 is greater than Vout 450 and neither converter phase 480 nor 481 is ON. In this case, HSON1 485 would be at logic zero and FET 412 would be ON thereby discharging capacitor 411 to substantially zero volts. Vref 417 would then cause the output of comparator 410 to transition to logic zero removing the reset from latch 409. If Vref 417 is also greater than Vout 450, then circuitry in PSL 482 would transition Start PH1 490 to logic one setting latch 409. Then, HSON1 485 transitions to logic one turning FET 407 ON via gate drivers 408. Current from Vin1 415 would start increasing Vout 450. When latch 409 is set, its complementary output 492 transitions to logic zero turning FET 412 OFF and allowing capacitor 411 to charge towards Vin1 415. When the positive input of comparator 410 exceeds Vref 417, the ON-time pulse (HSON1 485) for converter phase 480 terminates. Then, FET 406 turns ON and the current stored in inductor 404 circulates to Vout 450 via FET 406. Diode 405 provides a conduction path during the transient turn ON of FET 406. Amplifier 432 senses the current from converter phase 480 by the voltage across resistor 403. GMA 432 may be a voltage amplifier or a transconductance amplifier as explained relative to Figure 3. The output of GMA 432 is coupled to resistor 436. FET 407 is turned ON by signal 487, which also turns FET 439 ON . When FET 439 turns ON, it "samples" the output of GMA 432 by charging capacitor 438, which is coupled to the negative input of comparator 433. When FET 439 turns OFF, capacitor 438 holds this voltage which is representative of the peak current in converter phase 480 during its previous ON cycle. Capacitor 438 is coupled to the negative input of comparator 433. The output of comparator 433 is coupled to the reset input of latch 420 in converter phase 481. If there is yet no current from converter phase 481, then the current in resistor 435 is zero and the reset to latch 420 is logic zero.

Please replace the paragraph beginning on page 15, line 25 with the following:

When Start PH1 490 transitions to logic one, it clocks FF 461. Since FF 461 was initially reset, its negative output 496 is logic one. A positive input to the CLK of FF 461 sets its positive output 497 to the value of its D input. With this configuration, each time

the CLK of FF 461 transitions to logic one, the state of FF 461 flips to an opposite state. In this case, Q output 497 transitions to logic one. Positive transitions of output 497 are delayed by rising edge delay (RDL) 462. If Vref 417 is greater that Vout 450 (See Figure 4A), then when Start PH2 491 transitions to logic one converter phase 481 also ON. When Start PH2 491 transitions to logic one it clocks FF 450 via its CLK input. Since FF 450 was reset by positive pulse 460, it is again set and output 499 transitions to logic one. During initial ramp up of Vout 450, it will take several cycles before Vout 450 exceeds Vref 417, therefore, output 499 again transitions to logic one. If convert phase 480 has not turned OFF, latch 409 (See Figure 4A) will remain set. As soon as comparator 410 transitions to logic one, resetting latch 409, HSON1 485 transitions to logic zero triggering inverted pulse 456 which degates AND gate ~~456~~ 457 causing Start PH1 490 to transition low removing the set to latch 409 for a OFF blanking period equal to the pulse width of inverted pulse 456. At the end of inverted pulse 456, Start PH1 490 will again transition to logic one starting a new ON time for converter phase 480. Since converter phase 480 is turned ON with Start PH1 490 and turned OFF by a one shot timing circuit (FET 412, R 413, C 11, and comparator 410) it will continue to switch ON and OFF during initial ramp-up of Vout 450. Converter phase 481 turns ON with Start PH2 491 and does not turn OFF until its output current sensed via resistor 435 and GMA 434 is greater that the sampled peak value of the current in converter phase 480. Every time converter phase 480 turns OFF its current decays while the current from converter phase 481 continues increasing. When converter phase 480 turns back ON again it therefore supply less of the total load current to Vout 450. When Vout 450 exceeds Vref 417 the output of comparator 467 transitions to logic zero degating AND gate 468 and thus AND gates 455 and 465. Both converter phases are prevented from turning ON after they turn OFF due to Vout 450 exceeding Vref 417. When Vout 450 again drops below Vref 417, the output of comparator 467 transitions to logic one and the output of AND gate 468 transitions to logic one. This positive transition via OR gate 446 triggers positive pulse 447 to set FF 450 and reset FF 461 and the cycle will repeat until Vout 450 again exceeds Vref 417. Inverted pulse 464 and AND gate 466 operate in converter phase 481 as inverted pulse 456 and AND gate 457 in converter phase 480.

Please replace the paragraph beginning on page 17, line 4 with the following:

Figure [[4c]] 4C is a timing diagram of selected signals of circuit 400 in Figure 4B. These signals illustrate a key difference between embodiments of the present invention and the prior art. On a power-on-reset set pulse 469 initializes circuit 400 by setting latch 450 and resetting latch 461. During set pulse 469, AND ~~408~~ 468 is degated which in turn degates AND gates 455 and 465. When latch 450 is set, its Q output transitions to logic one. Rising edge delay 458 delays the positive transition of latch 450, which in turn delays the transition of Start PH1 490 to logic one. Start PH1 490 sets the ON-time latch of phase one (shown in Figure 4A) and HSON1 485 transitions to logic one. HSON1 485 triggers positive pulse 460 and resets D-latch 450. HSON1 485 remains logic one for the ON-time of phase one. The ON-time of phase one is determined by other circuitry in the controller for the regulator (See Figure 4A). Start PH1 490 clocks D-latch 461 when it transitions to logic one. Since D-latch 461 was initially reset, it now sets. After the rising edge delay ~~461~~ 462, Start PH2 491 transitions to logic one starting the ON-time for phase two. Since the ON-time of phase two is terminated only when the current in phase two equals a sampled current in phase one, HSON2 ~~495~~ 486 remains at logic one while HSON1 ~~490~~ 485 continues as a repetitive pulse. Prior art circuits have cross blanking circuitry that prevents both phases from being ON at the same time. The present invention allows both phase to be ON and thus has a faster transient response at start-up and during fast load changes. In some systems, the regulator input voltage for phase one is larger that for phase two (e.g., 12 volts and 5 volts). Using embodiments of the present invention the 12 volts of phase one can ramp the inductor current quickly whereas the 5 volts of phase two cannot because it presents much less voltage to charge the inductor when the high side FET (e.g., 418 of Figure 4A) is ON.